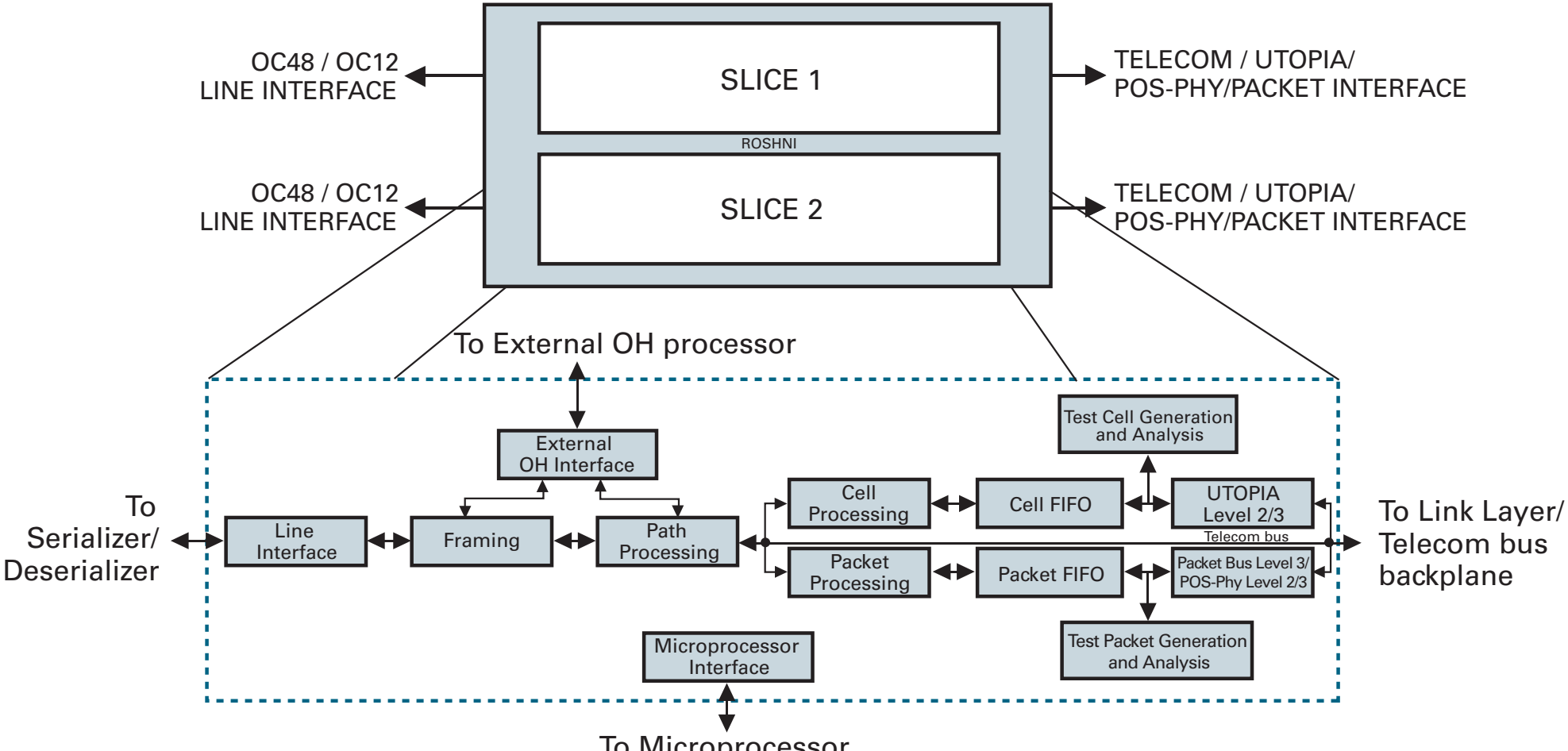
OC48 / OC12
LINE INTERFACE
SLICE 1
ROSHNI
SLICE 2
OC48 / OC12
LINE INTERFACE
TELECOM / UTOPIA/
POS-PHY/PACKET INTERFACE
TELECOM / UTOPIA/
POS-PHY/PACKET INTERFACE
To External OH processor
External
OH Interface
Test Cell Generation
and Analysis
To
Serializer/
Deserializer
Line
Interface
Framing
Path
Processing
Cell
Processing
Cell FIFO
UTOPIA
Level 2/3
Telecom bus
Packet
Processing
Packet FIFO
Packet Bus Level 3/
POS-Phy Level 2/3
To Link Layer/
Telecom bus
backplane
Microprocessor
Interface
Test Packet Generation
and Analysis
To Microprocessor